IN THE SPECIFICATION

Please Amend the paragraph beginning on page 10, line 4 in accordance with the following mark-up:

Depending on the relative resistance of transistor **N21** to shorting resistance **24**, shorting resistance **24** may or may not cause a logic level transmission fault to other logic circuits ~~**24**~~ **23A** (i.e., an incorrect logic state within other logic circuits **23A** for the low level logic state of the inverter due to too high a voltage at the inverter output caused by shorting resistance **24**.) In all cases, shorting resistance **24** causes a delay increase for the transition to the logic low state of the inverter. The above-described delay variation may cause a functional failure of die **12A**. If the resistance of shorting resistance **24** is relatively high with respect to the driving circuit resistance (i.e., the on state equivalent resistances of transistors **N21** and **P21**), then the delay variation will be negligible. The present invention provides a methodology for determining the relative resistance of a shorting resistance defect to the driving-point resistance without knowing where the fault is located, and thus permits selective rejection of dies based on the relative resistance rather than absolute current magnitude. Without the ability to determine relative resistance of a fault, an IDDQ test may falsely indicate a severe defect for high fault leakage current causing unacceptable rejection of functional dies or indicate a non-severe defect for low fault leakage current causing non-functional devices to pass an IDDQ test.

Please Amend the paragraph beginning on page 13, line 27 in accordance with the following mark-up:

Figure 4B depicts the first derivative of the IDDQ curves of **Figure 4A**. The peaks of each curve can be used as an approximation of the VDD point of onset of non-linearity. The bottommost curve **53** at the left of the graph (corresponding to the first derivative of curve **51** of **Figure 4A**) has a peak at approximately VDD = .9V, exemplifying a device for which the non-linear range is large. For some defects, the non-linear region may extend throughout the entire measured voltage interval, in which case no peak may be observed in the first derivative. The curve <u>52</u> having the leftmost peak corresponds to the top curve **50** of **Figure 4A**, and indicates an onset of non-linearity **54** at the lowest VDD voltage of any of the curves. The linear range indicated for curve **50** is thus the largest linear range; curve **51** has the smallest linear range. The VDD position of the peak of the first-derivative curve can be detected (by taking the second derivative or by other means) and used to determine a VDD range over which the IDDQ vs. VDD performance is linear. A threshold above which the IDDQ curve remains non-linear can then be used as a pass/fail threshold for rejecting dies. In general, a threshold will also be applied to the first derivative peak-detection algorithm, so that numerical or measurement noise does not cause a false indication of a change in linearity.